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Design of an array multiplier in PFSCL style

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Abstract

In intergreted circuit design, the current trend is to create circuits that work well for both digital and analog (mixed signal) applications. The PFSCL has been a optimum choice in these applications. This paper proposed three different architectures of 2-bit array multiplier in PFSCL style. The architecture-1 uses PFSCL NOR/OR gates, the architecture-2 uses PFSCL Fundamental cell (FC), and the last architecture-3 integrates memristors with PFSCL design circuit. All proposed architectures are simulated in LT Spice tool with 90nm PTM technology. Out of all the proposed architectures, architecture-3 observes the most efficient in all the performance parameter. The proposed architecture-3 observes maximum reduction of 39 %, 66 % in paramter like delay and power consumption respectively, additionally, offers a maximum area saving of 97 % as compared to proposed architecture-2.

Subject Classification: *94C11.*

Keywords: *Mixed-signal design, Digital circuits, PFSCL, Fundamental cell, Memristor.*

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1. Introduction

Advancements in fabrication have enabled the mixing of billions of components on a solo chip, enhancing performance and reducing costs. CMOS technology remains dominant in VLSI due to its high speed and low static power consumption [1-3]. However, scaling CMOS faces challenges, such as balancing power and speed, and addressing switching noise caused by significant current during transitions. These issues drive the need for alternative design approaches to support mixed-signal IC integration.

Researchers have explored alternative logic styles, with PFSCL system have analog and digital circuits fabricated on the same substrate being a suitable choice in mixed-signal environments due to its high-speed advantages [4-8]. PFSCL gates utilize a constant current source, ensuring stable power consumption, and various PFSCL circuits like adders, serializers, and flip-flops have been proposed [9-15]. However, multiplier designs in PFSCL remain unexplored. This paper focuses on efficient 2-bit array multiplier architectures in PFSCL, which multiply two 2-bit binary numbers to produce a 4-bit output [16-17]. Three architectures are introduced: using conventional PFSCL NOR/OR gates, PFSCL fundamental cells (FC), and memristors.

The paper has five sections. The first section introduce the benefits in the chosen logic style. An overview of 2-bit array multiplier and conventional PFSCL designs is presented in Section II. Section III presents the different

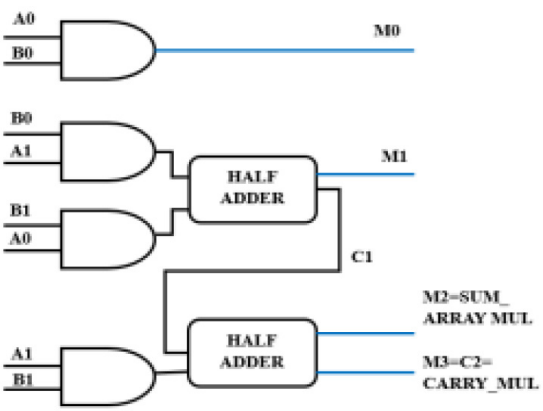


Figure 1

Block diagram of 2-bit array multiplier [16-18]

architectures of 2-bit array multiplier in PFSCL style. Following this, Section IV outlines the performance comparison and functional verification of all the proposed architectures through simulations using 90nm CMOS technology parameters. Lastly, conclusions are drawn in Section V.

2. Basic concepts

This section first briefly presents the concepts related to array multiplier. Thereafter, different schemes to realize PFSCL circuit is presented.

2.1 *Array (2-bit) Multiplier*

An array multiplier is defined in a digital circuit that performs multiplication via a grid of adders and AND gates. A 2-bit array multiplier consists of four AND gates and two half-adders, with carry values added sequentially, as shown in Fig. 1 (a) [16-18]. The whole method of a 2-bit array multiplier can be explained as: For a 2-bit array multiplier, with inputs A = A0A1 and B = B0B1, the product bits (M_3, M_2, M_1, M_0) are calculated as follows: The least significant bit (M (0)) is the result AND operation of A0 by B0. The next bit (M (1)) is obtained by first performing AND operation on (A1B0) and (B1A0). The output of these AND gates is further used for half adder operation to obtain the desired result at M1. This process is repeated for the remaining bits to complete the multiplication.

2.2 *PFSCL style*

Positive Feedback Source Coupled Logic) is a single-ended variant of Source Coupled Logic designed to enhance switching speed compared to traditional SCL implementations. A conventional PFSCL inverter, as illustrated in Fig. 2. It consists of load transistors, the pull-down network (PDN), and bias current source (I_{SS}). The PDN, implemented using transistors M_1 and M_F, is responsible for executing the logic operation. It directs the bias current (I_{SS}) through PDN branches. The PMOS transistors (MP_1) play a crucial role in converting the current into a voltage signal to produce required output. The operation of the PFSCL inverter, is described below:

For the input value (A) is low, I_{SS} flows through the M_F keeping V_{OH} ($V_{OH} = V_{DD}$). When a high A steers I_{SS} through M_1, making ($V_{OL} = V_{DD} - V_{SWING}$).

In the literature, three standard PFSCL configurations have been proposed to realize different using this style [7]. The first is the conventional PFSCL design approach which involves NOR/OR [6-7] gates, the second PFSCL design approach uses fundamental cell (FC) [15] while the third integrated memristor in PFSCL circuit design [18].

2.2.1 NOR/OR PFSCL design

The conventional PFSCL design employs only PFSCL NOR/OR gates. A generic PFSCL NOR/OR gate connects input transistors (A_1, ----A_N) in parallel and source-coupled them to a transistor M_F driven by the gate output as shown in Fig. 3 [6-7,15]. The conventional PFSCL based NOR/OR gates are used for the realization of complex logic functions which are typically built using a series of NOR/OR gates. To implement an XOR2 function, three 2-input gates are required. This PFSCL design approach can be extended to implement other complex functions, but it generally results in a high number of gate count. To improves the performance of PFSCL NOR/OR design another PFSCL design is suggested in [14].

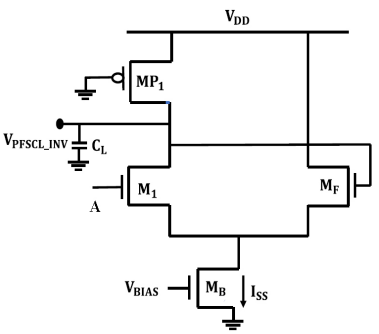


Figure 2
Conventional PFSCL Inverter [7]

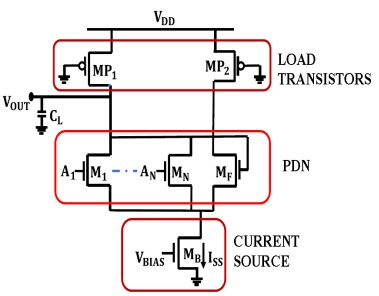
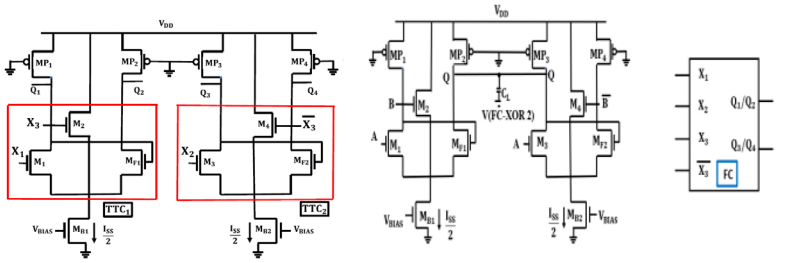


Figure 3
Gate level XOR2 gate [19]

2.2.2 PFSCL FC design

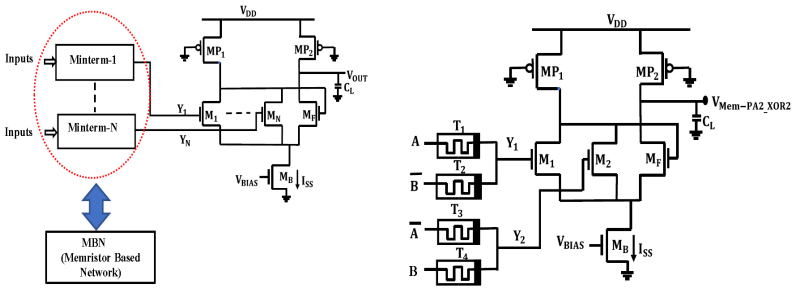
To address the problems with the PFSCL NOR/OR design, an alternative design has been suggested, which uses a FC in the PFSCL design [14,18]. A FC includes two triple-tail cells (TTCs) to implement functions involving two variables. Figure 4(a) shows the MOS-based diagram of a PFSCL FC. At a particular instance, only one TTC is active,



(a) (b) (c)

Figure 4

(a) Conventional Fundamental cell [13] (b) Symbol (c) FC based 2-input XOR



(a) (b)

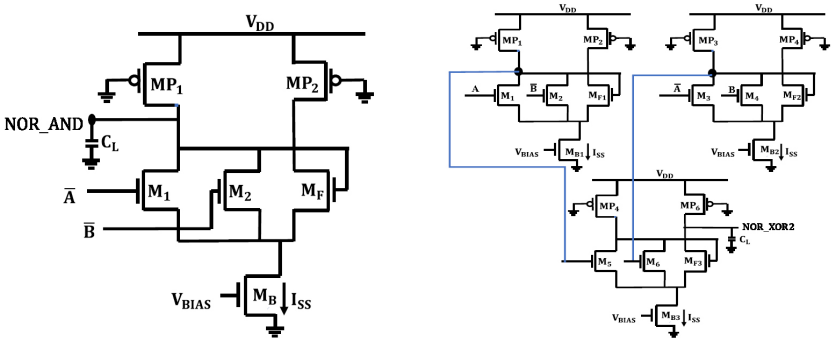
Figure 5

Memristor based design (a) Mem-PA2 [18] (b) XOR2 gate

while the other is turned OFF. For example, to implement an XOR2 function, input A drives to both X_1 and X_2, and X_3 is set to B. The outputs Q_1 and Q_4 from TTC_1 and TTC_2 are combined, as shown in Fig. 4(b) with its representative is shown in Fig. 4(c)). The conventional PFSCL FC in circuit design is observed to be more efficient than conventional PFSCL NOR/OR design because it reduces the number of cascade structure for complex function realization leading to lower current sources and overall low power consumption. However, it is important to note that PFSCL FCs require larger middle transistors in the TTCs, which increases the footprint of the PFSCL design and limits its flexibility for certain applications.

2.2.3 Memristor based PFSCL design

A new approach integrates memristors with PFSCL to enhance complex function designs as compared to Memristor-CMOS hybrid integrated circuits [20]. The Mem-PA1 method uses a memristor based



(a) (b)

Figure 6

(a) Proposed architecture-1 (a) AND gate (b) XOR2 gate

network in PFSCL style, while Mem-PA2 involves the memristor based network with NOR/OR gates in PFSCL style. It has been found that the Mem-PA2 design performs better than Mem-PA1, So, Mem-PA2 is the preferred method for further implementation. The block diagram for Mem-PA2 is shown in Fig. 5(a) [18]. The design of Mem-PA XOR2 function is shown in Fig. 5(b).

3. Proposed architectures

In this section, three different architectures of 2-bit array multiplier are proposed in PFSCL style. To build complex functions realization, this proposed architecture-1 requires a lot of PFSCL NOR/OR gates based AND and XOR as shown in Fig. 6(a) &(b).

3.1 *Proposed architecture-1*

The first realization employs a NOR/OR PFSCL design, utilizing four AND gates and two half adders to implement the 2-bit array multiplier. The half adder consists of a PFSCL NOR/OR-based carry circuit and an XOR2 gate formed with two NOR gates and one OR gate. To build complex functions realization, this proposed architecture-1 requires a lot of PFSCL NOR/OR gates. As a result, increased propagation additionally, reduce the speed benefits of the PFSCL style. So, to improve the performance of proposed architecture -1, another architecture is proposed in next section.

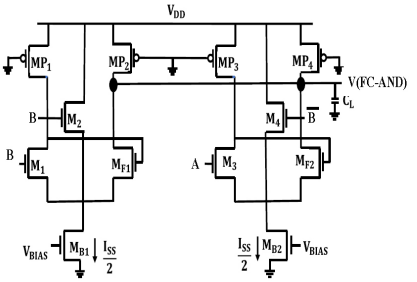


Figure 7
PFSCL FC AND gate

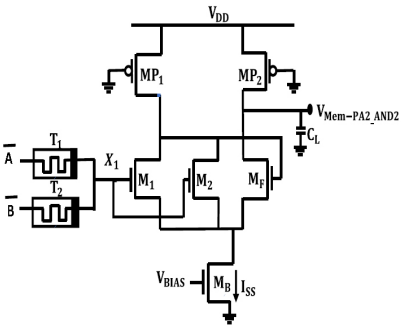


Figure 8
Mem-PA2 based AND gate

3.2 *Proposed architecture-2*

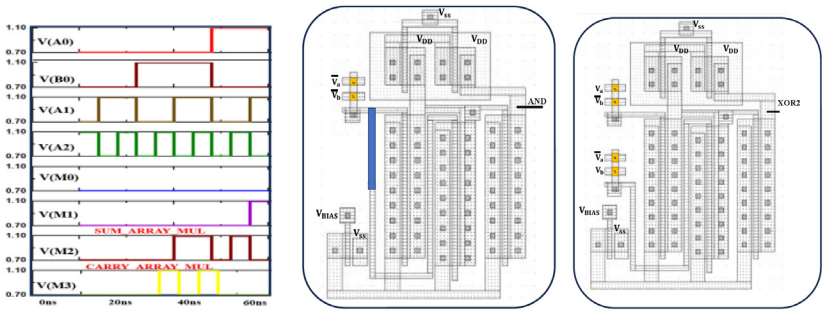
In this architecture-2 involves PFSCL fundamental cell-based design. For the implementation of AND function in PFSCL FC, connect input B to M_1, input A to M_3, and set M_3 to B and the output is obtained by combining outputs Q_2 from TTC_1 and Q_4 from TTC_2, as shown in Fig. 3(a). The same process is follows for implementation of XOR2 gate. This is more efficient than proposed architecture-1 due to reduced cascading which leads to low power consumption.

3.3 *Proposed architecture-3*

Architecture-3 utilizes the Mem-PA2 method, integrating a memristor-based network (MBN) within PFSCL NOR/OR gates for the 2-bit array multiplier. It requires fewer PFSCL gates compared to Architectures 1 and 2, minimizing gate count and area. This optimization significantly improves performance and efficiency of the PFSCL circuits. The same process is follows for implementation of AND gate as shown in Fig. 7.

4. Simulation Section

In this simulation section, the functionality of 2-bit array multiplier is verified and the performance of proposed architectures is compared in terms of in propagation delay, power, power delay product (PDP), gate count and area. All simulations environments are carried out using LT spice with 90 nm CMOS technology. The parameters involve with a voltage supply, current, load capacitance and voltage swing of 1.1V,100 μA, 50 fF,



(a) (b) (c)

Figure 9

(a) Timing waveform of proposed architecture -3 for 2-bit array multiplier

Table 1

Performance comparison for a 2-bit Array

Designs / Parameter	SUM_ARRAY_MUL			CARRY_ARRAY_MUL		
	Architecture-1	Architecture-2	Architecture-3	Architecture-1	Architecture-2	Architecture-3
Propagation Delay (ps)	1970	1785	1450	1630	1785	992
Gate count	11	6	6	6	6	2
Power (μW)	1100	660	660	660	660	220
PDP (fJ)	2167	1178.1	1089	1075.8	1178.1	218.24
Area (μm^2)	751	5490	320	331	5490	132

and 400 mV respectively. Layouts are put forward for area comparison are created using Microwind.

4.1 *Function verification*

The timing waveforms of proposed architecture-3 of 2-bit array multiplier is shown Fig. 8. The simulated waveform of the 2-bit array multiplier, illustrating the inputs (A0, B0, A1, A2) and their corresponding output (M0, M1, M2, M3). The following results can be made from the obtained results:

4.2 *Performance comparison*

The proposed architecture-3 achieves a significant improvement in propagation delay, reducing it by 26% in SUM_ARRAY_MUL and 39% in CARRY_ARRAY_MUL compared to architecture-1. This enhancement results from the elimination of multiple stages present in architecture-1, which otherwise increase delay. Additionally, architecture-3 demonstrates a substantial reduction in power consumption, with decreases of 40% and 66% in SUM_ARRAY_MUL and CARRY_ARRAY_MUL, respectively, due to its lower gate and current source count. These optimizations contribute to significantly reduced power-delay product (PDP) values. Furthermore, architecture-3 offers notable area efficiency, with a reduction of 94% and 97% in the area for SUM_ARRAY_MUL and CARRY_ARRAY_MUL, respectively. The simulated results are shown in table 1. The area layouts of the AND and XOR2 gates for architecture-3 are depicted in Figures 9(b) and 9(c), while the layouts of other architectures are omitted for brevity.

5. Conclusions

The mixed-signal PFSCL design style has become a preferred option for use in applications requiring high-speed, low-power digital circuits. In this paper, we introduce three distinct 2-bit array multiplier architectures based on the PFSCL approach. Architecture-1 employs PFSCL NOR/OR gates, while architecture-2 utilizes the PFSCL Fundamental Cell (FC). The third architecture, architecture-3, integrates memristors with the PFSCL circuit design. All three architectures were simulated using the LT Spice tool with 90nm PTM technology. Among the proposed designs, architecture-3 stands out as the most efficient across all key performance metrics, offering the highest speed along with the lowest power consumption and area, making it an ideal choice for resource-constrained applications such as high-performance computing and low-power embedded systems.

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