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Optimized vedic multiplier using low power 13T hybrid full adder

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Abstract

The research paper detects a modified version of the Vedic multiplier by using the sutras of Vedic mathematics by implementing a 13T hybrid full adder. A conventional multiplier is considered for comparative analysis of existing Vedic versions and a modified Vedic multiplier that better reflects the timing and usage of the device. This technology was developed and implemented by EDA. The proposed 13T hybrid full adder is achieved to reduce the static power consumption by 12.12 % and dynamic power consumption by 15.7%. The modified Vedic multiplier is implemented by using a 13T hybrid full adder which is achieved to reduce the power consumption by 10.08% and delay by 2.068%. The circuit and simulation are executed for 4-bit multiplication and can be performed in Eight-bit, Sixteen-bit or Thirty-two-bit. Results of simulation are shown only in the Vedic 4-bit multiplication technique. The results of this multiplication method are compared with existing techniques of Vedic multiplicative circuits.

Subject Classification: *68W35 Hardware implementations of nonnumerical algorithms (VLSI algorithm, etc.).*

Keywords: *Carry-save adder, Hybrid full adder, Vedic multiplier, Ripple carry adder.*

1. Introduction

Multiplication is commonly used for applications such as cryptography, IoT, processing of images and digital signal processing. Regular multipliers not only use more area but also have more latency. To enhance the enactment of the kernel or multiplier system, many complex algorithms and structures have been introduced. In a digital system, electronic processing system addition, multiplication, subtraction and

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division is the primary operation is required that is executed by adders, multipliers, subtractors and dividers respectively. [1] The hybrid full adder shows the expression of an improvement by analyzing the performance by comparing it with conventional adders. [8] The hybrid full adder is considered a noble way to improve the speed of operating performance as compared to other standard full adders circuits. Functionality, a bit low power hybrid FA (full adder) is designed and simulated using EDA tools & analyzed using settings of 5 volts and compared to waveforms and performance with different conventions full adders. [2-4]. To compare hybrid full adders with other standard full adders in various dimensions, such as the use of static power and dynamic power utilization is best for various applications. In this paper, we will show the application of our designed low power and energy-efficient adder by using it in Vedic multiplier and performance analysis with other conventional multipliers. 1-bit adder provides low energy integrated circuit provides low power delay due to low power supply and transistor size. Consequently, the limitation of that circuits is the high range & slow speed due to the achievability of positive MOS devices and the large involvement potential of gates due to a stable complement of complementary metal-oxide semiconductors. [5-7]. Adders show a significant role in numerous mathematics multiplier circuits. Swiftness and consumption of power become very important in power-saving design considerations of a multiplier.

In this paper, the Vedic multiplier has been designed using low power & energy-efficient 13T hybrid full adder that we designed by reducing the numbers of the transistor and modifying in the modules of 18T low power hybrid full adder as shown in Figure 1. The Vedic multiplier archives for this article are based on Vedic mathematical principles. Vedic mathematics

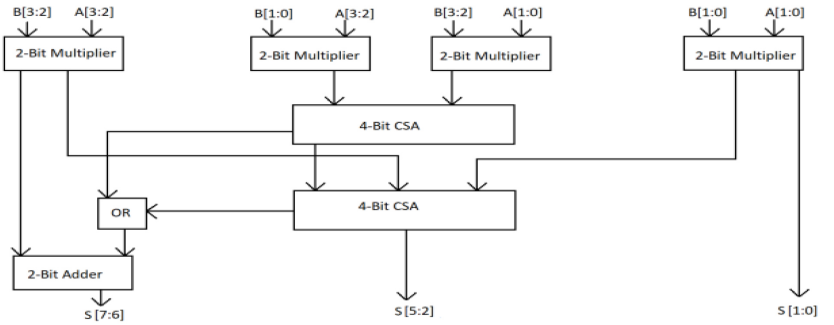


Figure 1

Block diagram vedic multiplier [1]

is part of the four Vedas and part of the ancient Indian mathematical system (books of knowledge). [1–2]. The meaning of Vedas is knowledge which has a derivational sense of principle and is the infinite storehouse of all knowledge. It has a special calculation technique founded on 16 sutras (formulas). It includes some modern math terms like geometry, arithmetic, trigonometry, factorization and quadratic equation. The execution of the Vedic multiplication algorithm for multiplication is grounded on the Urdhva Trikabhayam Sutra, a unique way of multiplication that is appropriate for every type of multiplication case [1].

2. Schematic design and simulation results

In this paper, the designed circuits are verified through TSPICE under the EDA Tool standard CMOS process and the simulated waveform is shown.

A. *Schematic Design of 13T Hybrid Full Adder*

The hybrid full adder architecture gains relatively less power and delay. Studies have shown that full adder designed in less PDP oriented CMOS perform better than the rest of most cells of conventional full adder which perform better by considering various loads on the supply voltage scale. Figure 2 shows the schematic design of 13T Hybrid full adder which take A, B and C as input of circuit and gives SUM and Cout as output of the circuit and the waveform for the given input is shown in Figure 3.

B. *Use of RCA in Vedic multiplier*

Figure 4 is schematic design of the ripple carry adder that is used in the execution of Vedic multiplier, full adders are configured in a format to produce the result of adding a n-bit string. Inputs for the next full addition phase are derived from addition by previous adder, addition performed in series until the final phase is reached. Figure 5 shows simulated waveform

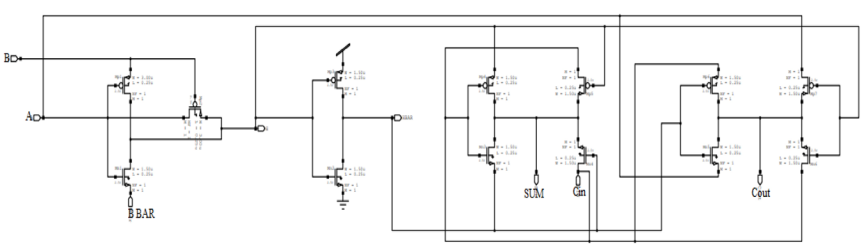


Figure 2

13T Hybrid full adder

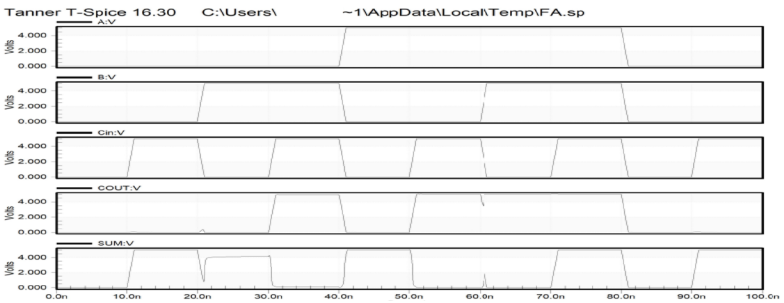


Figure 3

Output of 13T full adder

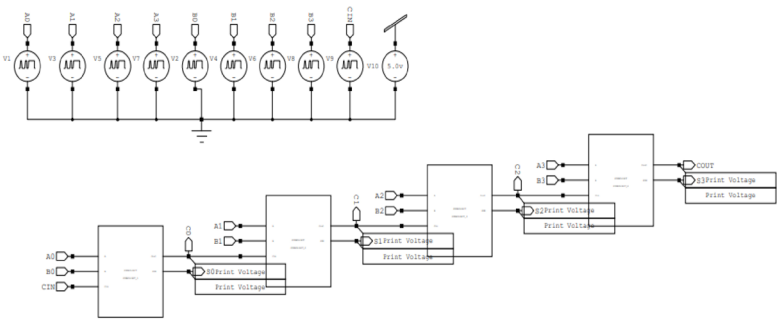


Figure 4

4-bit RCA

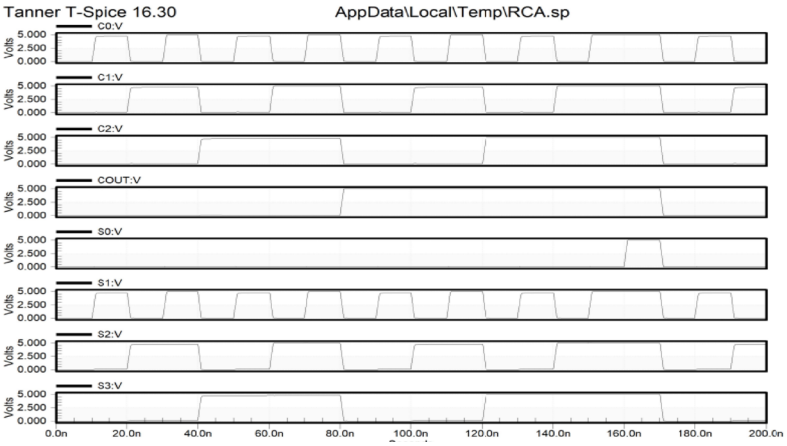


Figure 5

Output waveform of 4-bit RCA

of Four bit (RCA) Ripple Carry Adder. RCA is connected in such a way that output carry becomes the input carry for the next adder and output is derived as shown in Figure 5.

C. *Use of binary multiplier in Vedic multiplier*

A binary multiplier of 2 bit is designed by using 13T hybrid full adder for calculating the intermediate calculations and give the output of 4 bit as (C3-C2)(D3-D2) used in digital electronics in executions of various electronic circuits, like as in a computer of locating a product of 2-binary numbers. The deception of regular multiplication is used by the binary multiplier and multiply by each bit of the coefficient starting with the least significant bit 13T hybrid full adder (FA) modules are used. To perform a 2-bit binary multiplier as shown in Figure 6, not any computer arithmetic can use for the digital device multiplier factor. Figure 7 represents the simulated and verified output of the binary multiplier used in the Vedic multiplier.

D. *Use of carry-save adder (CSA) in Vedic multiplier*

The two parallel full adders that are used in the conventional Vedic multiplier are switched by CSA to implement the Vedic multiplier structure that is shown in Figure 8. It represents the design implementation of the carry-save adder (CSA) using 1-bit HFA and 4 bit RCA that leads to results S1 S2 S3 S4 which takes input from 2-bit multiplier when Vedic multiplier is implemented. Figure 9 represents the simulated waveform of the carry-save adder to verify the functioning of CSA.

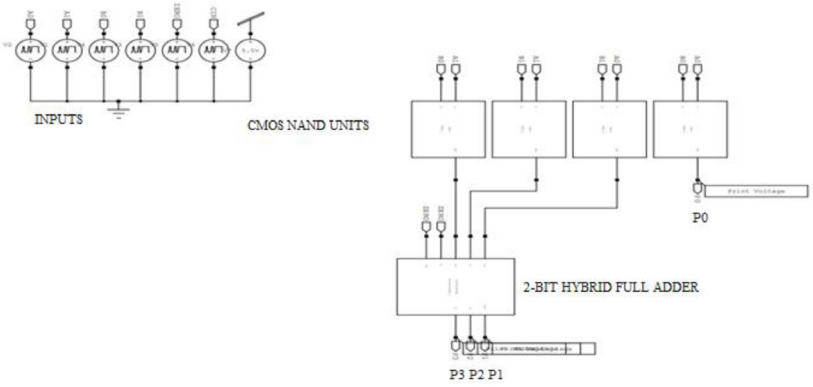


Figure 6

2-bit multiplier implementation using CMOS NAND units & 2 bit 13T hybrid full adder unit

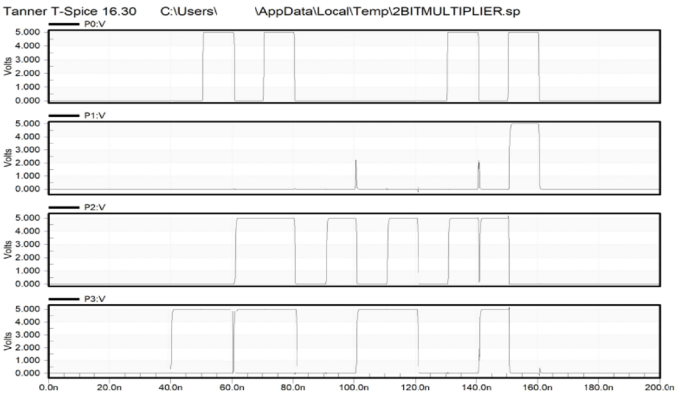


Figure 7

Output of 2-bit multiplier

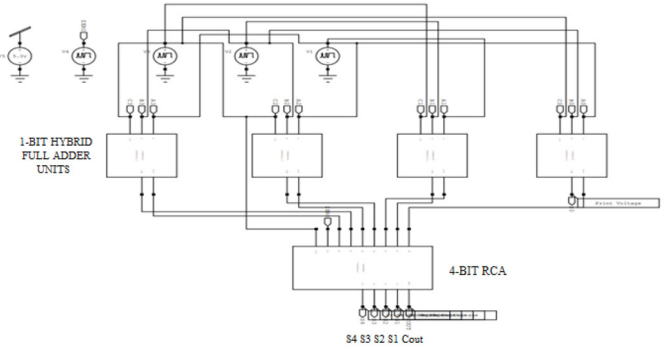


Figure 8

Carry select adder using 2-bit multiplier and 4-bit ripple carry adder

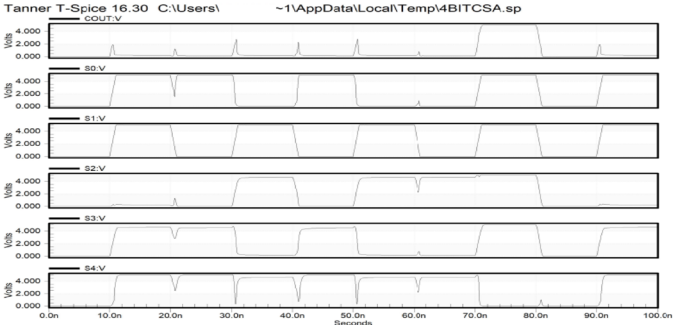


Figure 9

Output of carry-save adder

E. *4-BIT Vedic multiplier*

Initially, a four-bit modified Vedic multiplier utilizing 13T hybrid full adder is executed and similarly, the multiple bit design of the Vedic multiplier of 8 bit, 16 bit and then up to 32 bit can also be designed and implemented. In the same way 4 bit was designed using RCA. Using CSA, 4-bit Vedic modifier was applied and similarly, the range of a modified Vedic converter has been increased to 32-bit, such as 8, 16 and 32-bit [1]. Functional verification and simulation are done using the EDA tool. Figure 10 represents 2 full adders that are switched by using CSA to implement a multicore multiplier structure. The Vedic multiplication method is recommended to be performed on the following 4 input responses, C (C3 –C0) and D (D3 –D0) & eight outputs S (S0 –S7) in three data sets of 4: S20S21S22S23, S10S11S12S13 and S30S31.S02S03. 4-bit changed design Vedic multiplier is realized and executed. The end two Most Significant Bits are offered as input of CSA to OR gate. Along with this, the Ripple Carry Adder with a four-bit output terminal is being substituted with a 2-bit adder design circuit that can control the value of the output of the OR gate. An input of preceding stage 2-bit adder gets attained by the OR gate output.

$$
\begin{array}{lll}
 & C3C2C10 & \\
 & x\ D3D2D1D0 & \\
 & \overline{(C3C2)x(D1D0)} \quad (C1C0)x(D1D0) & \\
(C3C2)x(D3D2) & (C1C0)x(D3D2) & \\
\hline
S7\ \ S6 & S5\,S4\,S3\,S2 & S1\ \ S0
\end{array}
$$

3. Comparative analysis

Table 1

Comparison of static and dynamic of various adder circuit

Adder circuit	Static power	Dynamic power
CMOS [7]	372.0 pw	6.1416 µw
CPL [7]	1.379 nw	7.2183 µw
Hybrid CMOS 18T FA[4]	229.2 pw	2.7853 µw
Hybrid CMOS 13T FA	201.428 pw	2.3456 µw

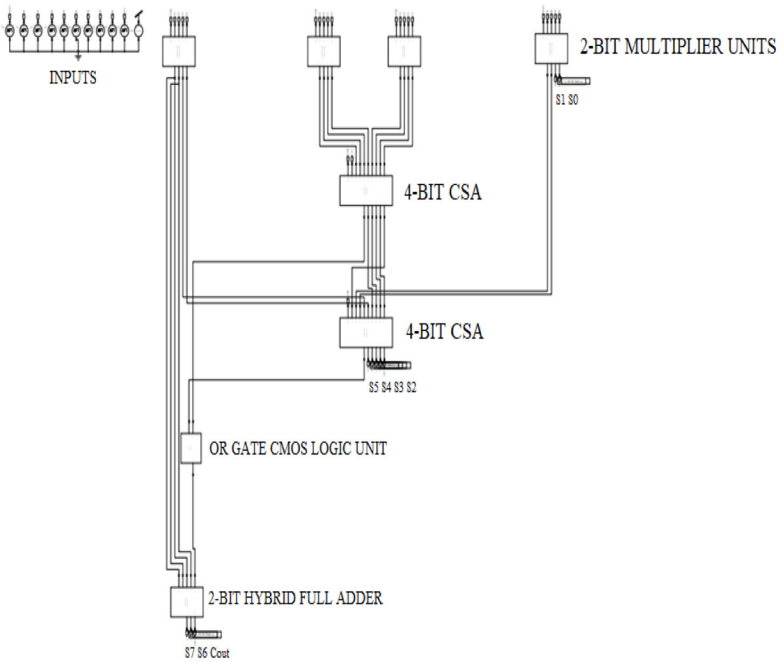


Figure 10

4-bit vedic multiplier using RCA, 4-bit CSA, or gate & 2-bit hybrid full adder and binary multiplier

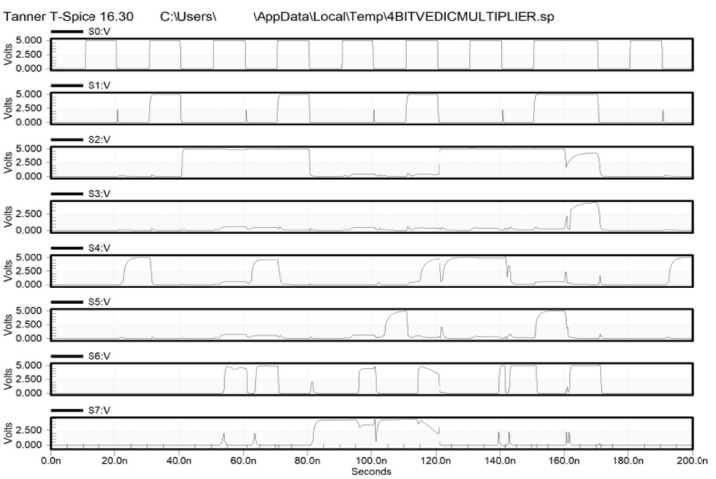
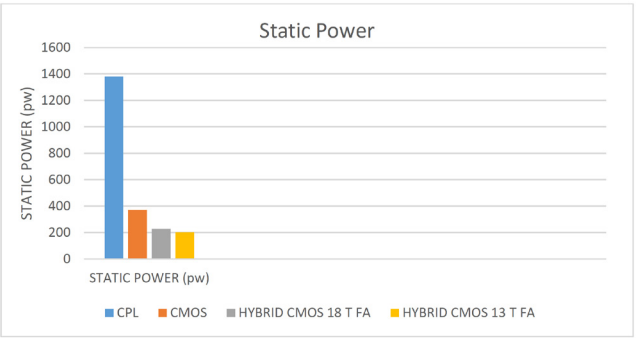
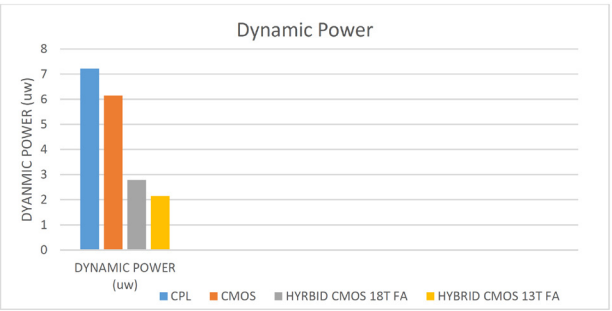


Figure 11

The output of 4- bit vedic modified multiplier using 13T hybrid full adder



(a)



(b)

Figure 12

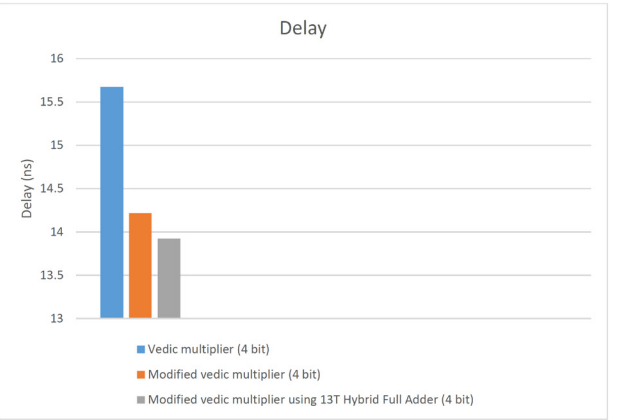
(a) Static power consumption (b) Dynamic power consumption

From Table 1 it is shown that static and dynamic power consumption of Hybrid CMOS 13T FA is reduce to 12.12 % and 15.7% respectively than the Hybrid CMOS 18T FA and also compares with CMOS and CPL logic FA that shows that consumption of static and dynamic power of Hybrid CMOS 13T FA circuit is very less. The power dissipation for modifies Vedic multiplier using 13T Hybrid full adder is shown in Table 2. This table compares the power consumption, Delay and LUT's result of conventional Vedic multiplier, modified Vedic multiplier and modified Vedic multiplier using 13T Hybrid FA. The figure 11 shows the the output of 4- bit vedic modified multiplier using 13T hybrid full adder and figure 12 shows the static and dynamic power consumption of the modified vedic multiplier.

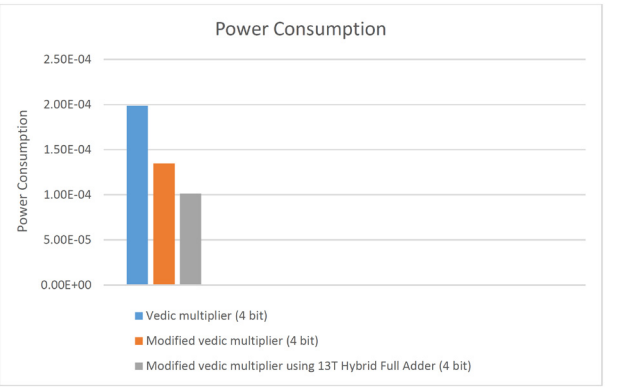
Table 2

Comparison of delay, power consumption and LUT's among various vedic multipliers

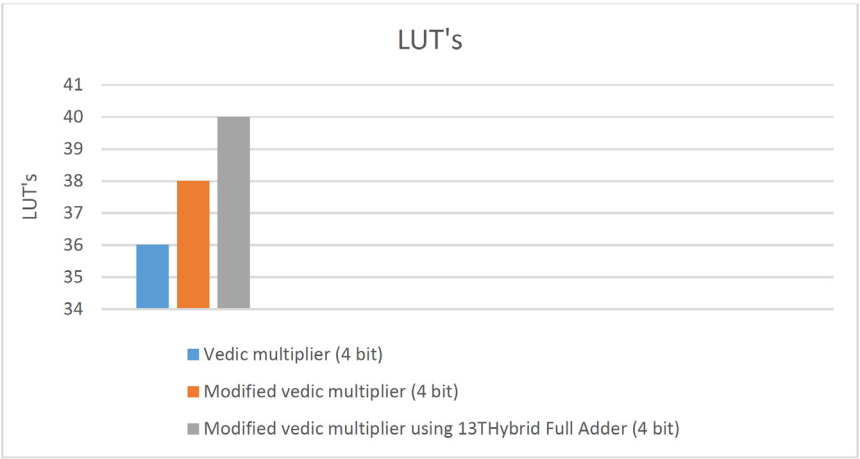
S.No	Multiplier	Delay (ns)	Power consumption	LUT's
1.	Vedic multiplier (4 bit) [1]	15.672	1.98593276e-004	36
2.	Modified Vedic multiplier (4 bit) [1]	14.215	1.12757901e-004	38
3.	Modified Vedic multiplier using 13T Hybrid Full Adder (4 bit)	13.921	1.01385167e-004	40



(a)



(b)



(c)

Figure 13

(a) Comparative analysis of delay various 4-bit vedic multiplier

(b) Comparative analysis of power consumption various 4-bit vedic multiplier

(c) LUT's utilization in various 4-bit vedic multipliers

From Table 2 it is shown that power consumption and the delay is reduced by 10.08% and 2.068% respectively when compared with modified Vedic multiplier and as modified Vedic multiplier using 13TFA is compared with conventional Vedic multiplier it is seen that power consumption is reduced to 48.94 % and delay is reduced to 11.17%. Figure 13 represents the comparative analysis of delay, power consumption and LuT's utilization among different vedic multiplier.

4. Conclusion

It is recommended that the system is more efficient in terms of delay and power utilization. Advanced bit rates can be achieved by utilizing the newly designed circuitry of the VLSI technology. In addition, various architectural additions may be used and in the design of the Carry Save Adder (CSA) utilized to change the Vedic coefficient. Among the numerous modified techniques, the design is used to enhance and accelerate the circuitry of a multiplicative system by using a modified Vedic multiplier using a 13T hybrid full adder. It is shown that power consumption and the delay is reduced by 10.08% and 2.068% respectively when compared with modified Vedic multiplier and as modified Vedic multiplier using 13TFA

is compared with conventional Vedic multiplier it is seen that power consumption is reduced to 48.94 % and delay is reduced to 11.17%.

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