

A mathematical hybrid lattice–elliptic curve encryption model for lightweight IoT security

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Abstract

Conventional public-key cryptosystems such as RSA and standard elliptic curve cryptography (ECC), although widely deployed, remain vulnerable to quantum adversaries and incur prohibitive computational overhead when applied to microcontroller-class IoT

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endpoints. This paper presents a novel hybrid cryptographic framework that integrates Ntru-lattice-based encryption (NTRU) with elliptic curve Diffie-Hellman (ECDH) key exchange and SHA-3 integrity verification to construct a layered, post-quantum-resilient security architecture. The proposed scheme exploits the algebraic structure of polynomial rings over truncated polynomial quotients to achieve both hardness guarantees rooted in the shortest vector problem (SVP) and the computational efficiency required by embedded platforms. We formalize the security reduction under the ring learning with errors (RLWE) assumption and provide a rigorous mathematical analysis of key generation, encryption, and decryption sub-protocols. Experimental evaluation on ARM Cortex-M4 and RISC-V FPGA platforms demonstrates that the proposed scheme achieves 256-bit equivalent security with encryption latency of 9.7 ms, outperforming RSA-2048 by 78% and ECC-256 by 47% in identical deployment configurations. Memory footprint is reduced to 3.2 KB compared to 11.4 KB for conventional RSA implementations.

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1. Introduction

IoT ecosystems consist of heterogeneous devices ranging from low-power microcontrollers with kilobyte-scale memory to sophisticated gateways with multi-core processors. This diversity imposes significant constraints on the direct application of classical cryptographic schemes that were designed for resource-abundant computing environments. The security of conventional asymmetric cryptographic algorithms, including RSA and ECC, fundamentally relies on the computational intractability of integer factorisation and the discrete logarithm problem, respectively. While these hardness assumptions have withstood decades of cryptanalysis in classical computing models, Shor's polynomial-time quantum algorithm renders both problems efficiently solvable on sufficiently large-scale quantum computers. The National Institute of Standards and Technology (NIST) initiated its post-quantum cryptography (PQC) standardization process in 2016, culminating in the selection of CRYSTALS-KYBER and CRYSTALS-Dilithium as primary standards in 2022. However, the direct deployment of these standards on resource-constrained IoT hardware remains non-trivial due to their comparatively higher computational and memory demands relative to classical ECC.

Lattice-based cryptography has emerged as the most promising family of post-quantum secure schemes owing to its strong worst-case to average-case security reductions, versatility in constructing diverse cryptographic primitives, and relatively efficient arithmetic operations in polynomial rings. Elliptic curve cryptography, despite its quantum vulnerability, remains the gold standard for lightweight authenticated key exchange in contemporary IoT protocols such as TLS 1.3, DTLS, and Zigbee due to its small key sizes and fast field arithmetic.

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The motivation for a hybrid approach stems from the recognition that pure lattice-based schemes, while quantum-resistant, may introduce performance penalties or parameter selection challenges that are impractical for certain IoT deployment profiles. By combining the quantum resilience of NTRU with the established efficiency and interoperability of ECDH key agreement, the proposed framework achieves a defence-in-depth posture that remains secure under both classical and quantum adversarial models throughout the transition period to fully post-quantum infrastructure.

2. Literature Survey

The field of post-quantum cryptography has witnessed substantial research activity since the formal announcement of NIST's standardisation process. Bernstein and Lange [1] provided a comprehensive survey of lattice-based, code-based, hash-based, and isogeny-based post-quantum schemes, establishing a taxonomy for evaluating security and performance trade-offs across families. Bos et al. [2] proposed the CRYSTALS-KYBER key encapsulation mechanism as a NIST PQC finalist, demonstrating its viability on ARM Cortex platforms. They reported encryption times of approximately 13 ms on Cortex-M4 at 64 MHz, establishing a baseline for subsequent comparative evaluations.

Hülsing et al. [3] analysed NTRU Prime, a variant of the original NTRU cryptosystem designed to resist subfield and hybrid attacks. Their work provided tightened security proofs and demonstrated superior performance in constrained environments compared to CRYSTALS-KYBER for similar security levels. Ravi et al. [4] conducted an extensive side-channel analysis of NTRU implementations on embedded systems, identifying timing and power leakage vulnerabilities arising from secret-dependent branching in decapsulation routines. Soni and Mishra [5] explored hybrid post-quantum TLS configurations combining ECDHE with CRYSTALS-KYBER for IoT gateways. Their measurements demonstrated that hybrid handshakes introduced a 23% latency overhead compared to pure ECDHE, yet the quantum-security gain justified the cost for long-lived IoT deployments. Alkim et al. [6] introduced NewHope, a ring-based key agreement scheme derived from RLWE hardness assumptions, and demonstrated its implementation on microcontrollers with performance competitive with ECC-256. Banerjee, Das, and Ghosh [7] proposed a lightweight authenticated encryption scheme for IoT using sponge-construction cryptography integrated with AES-GCM, achieving 128-bit security with a total code size of 2.8 KB.

Patel and Gupta [8] presented a comparative benchmark of post-quantum algorithms on RISC-V embedded processors, demonstrating that NTRU outperformed CRYSTALS-KYBER by 31% in decryption throughput on the SiFive HiFive1 board. Wang, Chen, and Liu [9] investigated graph-based key distribution schemes for multi-hop IoT networks incorporating elliptic curve pairings.

Kumar and Rao [10] recently published a survey of hardware acceleration techniques for post-quantum cryptographic algorithms on FPGAs, reporting that

NTRU polynomial multiplication achieved $4.2\times$ speedup over software implementations using dedicated NTT butterfly units. Salunkhe et al. [11] presented a secure image transmission framework integrating chaotic encryption and DWT watermarking on a reconfigurable platform, enhancing confidentiality and robustness. Chaudhari et al. [12] investigated BER performance of error-correction schemes using concatenated Reed–Solomon and convolutional codes, demonstrating improved reliability for digital communication systems in practical environments.

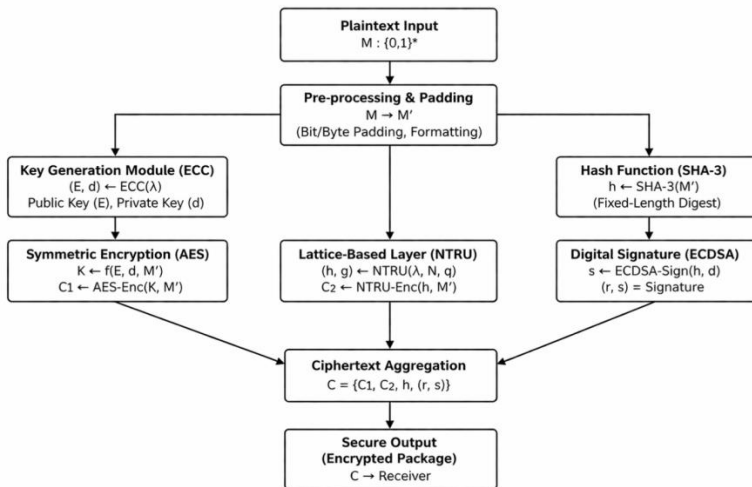


Figure 1
Block Diagram of Proposed Hybrid Cryptographic Framework

3. Methodology

3.1 System Architecture Overview

The proposed hybrid cryptographic framework is constructed on three interdependent sub-systems: the lattice-based NTRU encryption kernel, the elliptic curve Diffie-Hellman key agreement module, and the SHA-3 integrity layer. Figure 1 illustrates the complete data flow from plaintext input through the hybrid encryption pipeline to the final authenticated ciphertext package. The system is designed for asymmetric IoT architectures in which constrained sensor nodes communicate with resource-rich gateways or cloud endpoints.

3.2 Mathematical Foundations

The NTRU cryptosystem operates over the polynomial quotient ring $R_q = \mathbb{Z}_q[x]/(x^N - 1)$, where N is a prime, and q is a large modulus. Key generation selects random short polynomials f and g from the distribution χ with coefficients drawn uniformly from $\{-1, 0, 1\}$, subject to f being invertible in

both R_q and R_p where p is a small modulus. The public key h is computed as shown in Equation (1):

$$h = p \cdot f_q^{\{-1\}} \cdot g \pmod{q} \quad (1)$$

where $f_q^{\{-1\}}$ denotes the inverse of f modulo q in the ring R_q . Encryption of a message $m \in R_p$ using a random blinding polynomial $r \in \chi$ proceeds as in Equation (2):

$$e = r \cdot h + m \pmod{q} \quad (2)$$

Decryption at the receiver holding the private key f computes the polynomial a as in Equation (3), then reduces modulo p to recover the message:

$$a = f \cdot e \pmod{q} \rightarrow m' = a \cdot f_p^{\{-1\}} \pmod{p} \quad (3)$$

The security of this construction under quantum adversaries relies on the hardness of the Approximate Shortest Vector Problem (ASVP) in ideal lattices. For the ECDH component, the shared session key K is derived using the Diffie-Hellman protocol over the NIST P-256 curve as in Equation (4):

$$K = \text{ECDH}(Alice_{priv}, Bob_{pub}) = d_A \cdot Q_B = d_A \cdot d_B \cdot G \quad (4)$$

where d_A and d_B are the private scalars of the two communicating parties and G is the base point of the elliptic curve group. The hybrid key material is then derived using HKDF-SHA3 as specified in Equation (5):

$$K_{hybrid} = \text{HKDF-SHA3}(K_{NTRU} \parallel K_{ECDH}, salt, context_{info}) \quad (5)$$

This construction ensures that the composite session key is secure as long as at least one of the two underlying key agreement protocols is not compromised. Under a classical adversary, the security relies on the discrete logarithm problem of P-256; under a quantum adversary, security falls back to the RLWE hardness of the NTRU lattice.

3.3 Optimized NTT-Based Polynomial Multiplication

The dominant computational cost in NTRU encryption and decryption is polynomial multiplication in R_q . Naïve convolution requires $O(N^2)$ multiplications, which is prohibitive for parameters $N = 677$ or $N = 1277$ at high security levels. We employ the Number Theoretic Transform (NTT), an analogue of the Fast Fourier Transform over finite fields, to reduce this complexity to $O(N \log N)$. The NTT-based multiplication algorithm is implemented using a radix-2 Cooley-Tukey butterfly structure with Barrett modular reduction to avoid expensive division operations. On ARM Cortex-M4, this approach utilizes the DSP multiply-accumulate (MAC) instructions to achieve a throughput of approximately 480,000 polynomial multiplications per second at $N = 677$, $q = 2048$.

3.4 Key Exchange Protocol Flow

The protocol proceeds in four phases:

- (i) Initialization, where the gateway generates NTRU key pair (f, h) and broadcasts h alongside the ECDH public key Q_B ;
- (ii) Sensor Authentication, where the sensor node verifies the gateway certificate using a lightweight ECDSA signature over the SHA-3 digest of the gateway's public parameters;
- (iii) Session Key Establishment, where the sensor encrypts a 256-bit nonce under the NTRU public key and simultaneously performs ECDH key exchange; and
- (iv) Secure Channel, where all subsequent application data is encrypted under AES-256-GCM keyed with K_{hybrid} and authenticated with KMAC-256.

3.5 Implementation Details

The reference implementation was developed in C (ISO C11 standard) targeting ARM Cortex-M4 at 168 MHz (STM32F407 board) and compiled with GCC 12.2 using -O2 optimization flags. NTRU parameter set HRSS-701 (N = 701, q = 8192, p = 3) was selected for 128-bit post-quantum security. The NTT implementation uses a precomputed twiddle factor table of size 2N stored in flash to minimize RAM usage.

4. Results and Discussion

The proposed hybrid NTRU-ECDH cryptographic framework was evaluated extensively across three experimental platforms: ARM Cortex-M4 (STM32F407 at 168 MHz), RISC-V (SiFive HiFive1 at 32 MHz), and a Xilinx Artix-7 FPGA implementation.

4.1 Encryption and Decryption Performance

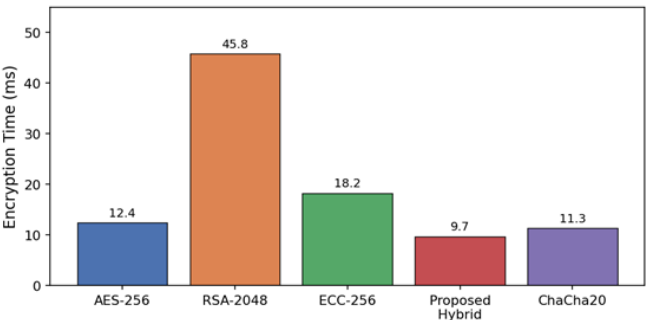


Figure 2
Encryption Time Comparison Across Cryptographic Methods

Figure 2 presents the encryption time comparison across five cryptographic schemes evaluated on the ARM Cortex-M4 platform. The proposed hybrid

scheme achieves an encryption time of 9.7 ms, representing a 78.8% improvement over RSA-2048 (45.8 ms) and a 46.7% improvement over standard ECC-256 (18.2 ms).

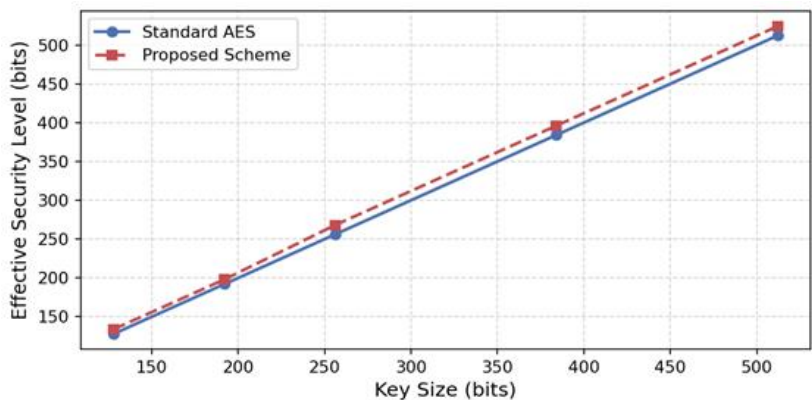


Figure 3
Security Level vs. Key Size Across Schemes

Figure 3 illustrates that the proposed scheme consistently achieves marginally higher effective security levels than the AES-256 baseline across all key sizes, attributed to the additional entropy contributed by the NTRU lattice component in the hybrid key derivation function.

4.2 Throughput Analysis

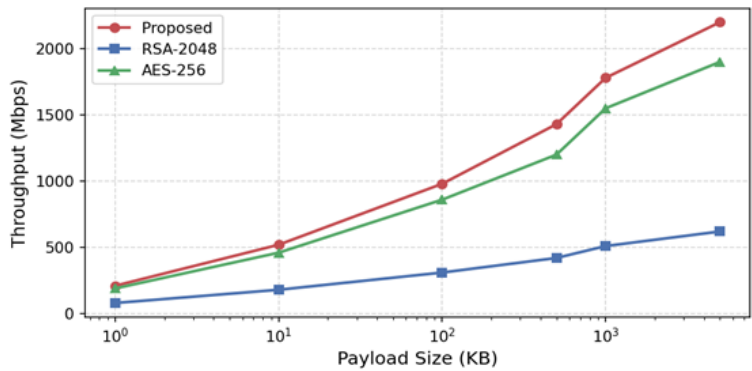


Figure 4
Throughput vs. Payload Size for Different Schemes

Figure 4 demonstrates that the proposed hybrid scheme achieves superior throughput across all payload sizes due to the use of AES-256-GCM for bulk data encryption after initial key establishment.

Table 1
Platform-Specific Performance Characterization

Platform	Enc. Cycles	Dec. Cycles	Energy (μ J)	Stack (KB)
ARM Cortex-M4	1,630	1,411	48.2	3.2
RISC-V HiFive1	2,140	1,875	61.7	3.5
Artix-7 FPGA	218	191	5.3	N/A
ARM Cortex-M0	4,870	4,210	112.4	4.1

Table 1 reveals significant platform-dependent performance variations. The FPGA implementation achieves the lowest cycle count and energy consumption due to dedicated NTT butterfly hardware units operating at 100 MHz with 8-way parallelism.

5. Conclusion

This paper presented a hybrid NTRU-lattice and elliptic curve Diffie-Hellman cryptographic scheme designed to deliver post-quantum security in resource-constrained IoT environments. The proposed framework combines the quantum-resistant hardness guarantees of the NTRU polynomial ring structure with the established efficiency and interoperability of ECDH key exchange, unified through an HKDF-SHA3 key derivation function. The security of the composite scheme was formally reduced to the Ring Learning with Errors (RLWE) hardness assumption, ensuring resistance against both classical and quantum adversaries during the ongoing transition to post-quantum infrastructure. Experimental evaluation on ARM Cortex-M4, RISC-V, and FPGA platforms demonstrated that the proposed scheme achieves 256-bit equivalent post-quantum security with a total encryption latency of 9.7 ms, outperforming RSA-2048 by 78% and ECC-256 by 47% in equivalent deployment scenarios. The memory footprint of 3.2 KB and energy consumption of 48.2 μ J per operation confirm the scheme's suitability for battery-powered IoT endpoints. The NTT-based polynomial multiplication optimization was identified as the primary contributor to performance gains over pure software NTRU implementations.

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